CLAIMS

1. (Currently amended) An imaging system comprising an image sensor, a memory, and a processor, wherein:

the image sensor is configured to generate image signals corresponding to an image of a scene;

the processor is configured to control operations of the imaging system in one or more operating modes enabled by one or more configurations accessible by the processor; and

the memory is configured to store the one or more configurations accessed by the processor to control the operations of the imaging system, wherein the imaging system further comprises interface pins, wherein a voltage pattern applied to the interface pins determines which of the one or more configurations is accessed by the processor.

2. (Original) The invention of claim 1, wherein:

the image sensor, the memory, and the processor are implemented as an SOC in a single integrated circuit;

the image sensor is a digital pixel sensor that generates digital image signals for storage in the memory; and

the memory is further configured to store image data corresponding to the image signals.

3. (Canceled)

4. (Original) The invention of claim 1, wherein the one or more configurations are stored in the imaging system.

5. (Original) The invention of claim 1, wherein the processor is configured to access at least one of the configurations from an external source.

6. (Original) The invention of claim 5, wherein the imaging system is configured to add from the external source new software corresponding to a new operating mode.

7. (Original) The invention of claim 1, wherein the imaging system is configured to operate in a still camera mode and a video camera mode.

8. (Original) The invention of claim 7, wherein the imaging system is further configured to operate in a troubleshooting operating mode.

9. (Currently amended) A method for fabricating an imaging system comprising the steps of:

(a) forming an image sensor;

(b) forming a memory; and

(c) forming a processor, wherein:

the image sensor is configured to generate image signals corresponding to an image of a scene;

the processor is configured to control operations of the imaging system in one or more operating modes enabled by one or more configurations accessible by the processor; and

the memory is configured to store the one or more configurations accessed by the processor to control the operations of the imaging system, wherein the imaging system further comprises interface pins, wherein a voltage pattern applied to the interface pins determines which of the one or more configurations is accessed by the processor.

10. (Original) The invention of claim 9, wherein:

the image sensor, the memory, and the processor are implemented as an SOC in a single integrated circuit;

the image sensor is a digital pixel sensor that generates digital image signals for storage in the memory; and

the memory is further configured to store image data corresponding to the image signals.

11. (Canceled)

12. (Original) The invention of claim 9, wherein the one or more configurations are stored in the imaging system.

13. (Original) The invention of claim 9, wherein the processor is configured to access at least one of the configurations from an external source.

14. (Original) The invention of claim 9, wherein the imaging system is configured to operate in a still camera mode and a video camera mode.

15. (Original) A method of operating an imaging system, the imaging system comprising an image sensor, a memory, a processor, and interface pins, the method comprising the steps of:

(1) applying a voltage pattern to the interface pins; and

(2) accessing a configuration corresponding to the voltage pattern, wherein:

the image sensor is configured to generate image signals corresponding to an image of a scene;

the processor is configured to control operations of the imaging system in one or more operating modes, wherein the accessed configuration enables at least one of the operating modes; and

the memory is configured to store one or more configurations accessible by the processor.

16. (Original) The invention of claim 15, wherein the voltage pattern applied in step (1) corresponds to logical "0" and logical "1" values.

17. (Original) The invention of claim 15, wherein the configuration accessed in step (2) is stored in the imaging system.

18. (Original) The invention of claim 15, wherein step (2) comprises the step of accessing the configuration from an external source.

19. (Original) The invention of claim 18, wherein step (2) further comprises the step of receiving the configuration from the external source for storage in the imaging system.

20. (Original) The invention of claim 15, further comprising the steps of:

(3) applying different voltage pattern to the interface pins; and

(4) changing operating mode.